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| --- | --- | --- | --- |
| Mike 2 | DS? | Chip | Mike 1 Design |
| 74273 x 2 | X | Octal D Type FlipFlop | One latches DL … might be IRQ Save ? |
| 7410 | X | 3 x 3 Input NAND | Status Decoding |
| 7404 | X | Hex Inverter | Clock Generator |
| 8T28 | X | Bus transceiver | *Added because of bus levels ?* |
| 74241 x 2 (not present) | X | Tristate Octal Buffers/Drivers | *Optional Input Ports* |
| 7400 | X | Quad 2 Input NAND | General Decoding |
| 7474 | X | Dual D |  |
| 74LS08 | X | Quad And gates | General Decoding |
| 8008 | X | CPU | Processor |
| 3205 | X | 3-8 Decoder | Figures out status |
| 7474 | X | Dual D |  |
| 7474 | X | Dual D |  |
| 7493 | X | 4 bit Binary Counter | Clock Generator (as 4) |
| 1702A | X | PROM 256x8 |  |
| 2112 | X | SRAM 256x4 |  |
| COM2017 | X | UART |  |
| 8T26 | X | Bus transceiver |  |
| 2102 | X | 1k x 1 RAM |  |
| 9368 | X | Hexadecimal Decoder |  |